

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Satwant Singh; Cyrus Tsui
Assignee: Lattice Semiconductor Corporation
Title: Delay-Matched ASIC Conversion Of A Programmable Logic Devices
Application No.: 10/660,814 Filing Date: September 12, 2003
Examiner: Daniel D. Chang Group Art Unit: 2819
Docket No.: M-15198 US Confirmation No.: 7052

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1) Response to Election/Restriction Requirement (1 page).

Dated: January 28, 2005


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Number of pages (including this sheet): 2

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RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Dear Sir:

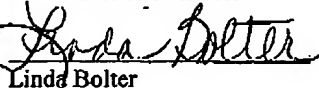
In response to the Restriction Requirement dated January 4, 2005, Applicants hereby elect to prosecute Group I, Claims 1-13, 17-20, and 32-37, without traverse.

Applicants reserve the right to prosecute non-elected Claims 14-16 and 21-31 in a divisional application.


If the Examiner has any questions, please call the undersigned at (949) 752-7040.

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Respectfully submitted,


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